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(54) **Apparatus for recording digital signals by controlling frequency characteristics of digital signals.**

(57) When modulating by interleaved NRZI by inserting one bit per every m bits of input data series, the frequency characteristics of bit rows varying by the polarity ("0" or "1") of the bit to be inserted are compared. and the bit row closer to the desired frequency characteristic is selected as the output series, so that recording is effected by controlling the frequency characteristics of the digital signal.

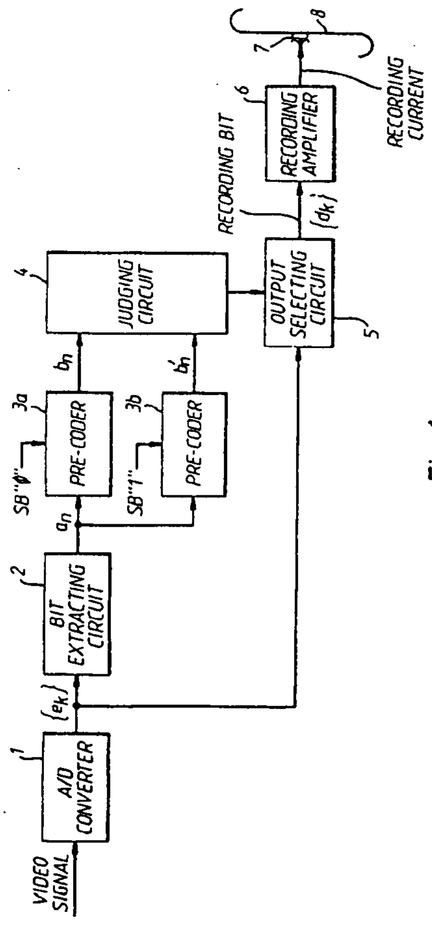

Fig.1

EP 0 593 173 A2

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The present invention relates to a recording apparatus for recording digital signals such as digital video cassette recorder (VCR).

In a magnetic recording apparatus such as VCR, when reproducing, as the head goes off the track, the head output is lowered, and the error increases, so that an accurate picture cannot be reproduced. It is therefore important that the head traces the intended track accurately, that is, to keep the head tracking. In the digital VCR for home use, in particular, the tracks are narrow in order to record a long time program, and it is required to keep the head tracking more accurately.

As the means for detecting deviation of the head from the track, making use of pilot signals between tracks, the crosstalks of the pilot signals from the preceding and succeeding tracks are compared, and it is detected that the head tracking is deviated to the preceding side or to the succeeding side.

The recording signals for this purpdse are modulated when recording so as to have frequency characteristics of three patterns F0, F1, F2 as shown in Fig. 22. In F0 pattern, frequencies f_1 and f_2 possess portions of small frequency components, that is, notch portions. In F1 pattern, frequency f1 possesses a portion of larger frequency components, that is, a pilot signal, while frequency f_2 possesses a notch portion. In F2 pattern, frequency f_1 possesses a notch portion, and frequency f_2 a pilot signal.

The recording signals are modulated so that the patterns may be in the order of F0, F1, F0, F2 as shown in Fig. 23, and recorded. When reproducing F0 pattern, by the crosstalk of pilot signals from F1, F2 patterns of adjacent track, there is a peak in frequency components of f_1 and f_2. When the head is deviated from the center of F0 pattern and is shifted to the F1 pattern side, the crosstalk of the pilot signal from F1 pattern becomes larger than the cross-talk from F2 pattern, and therefore the frequency components of f_1 of reproduced signal increase, while frequency components of f_2 decrease. Thus, by comparing the frequency components of f_1, f_2 of reproduced signals of F0 pattern, the deviation of head tracking can be detected, and a correct tracking is realized.

Hitherto, such patterns of F0, F1, F2 are formed by controlling the linkage of "0" and "1" in the binary series to be recorded. This method is explained below. First, the input data is divided by every m bits (m: an even number), and a "0" bit is added to the beginning of the m bits to enter a pre-coder to be modulated by interleaved NRZI (Non Return to Zero Invert). Similarly, a "1" bit is added to the beginning of m bits of the input data to enter the pre-coder to be modulated by interleaved NRZI. The characteristic of the pre-coder is expressed in formula (1), and it is utilized for known partial response detection when decoding, and moreover when the polarity of the bit to be inserted is inverted, the inversion of polarity is propagated as shown in formula (1), and it causes to increase the change of frequency characteristic by the change of polarity of the bit to be inserted. The bit of "0" or "1" to be inserted is hereinafter called a special bit (SB).

$$f_k = g_k + f_{k-2} \; (+ \text{ is exclusive OR}) \quad (1)$$

where $\{g_k\}$ is a pre-coder input data series, and $\{f_k\}$ is a pre-coder output data series. Extracting the frequency components of pre-coder output, the frequency components are compared between the pre-coder output when the SB is "0", and the pre-coder output when the SB is "1", and the pre-coder output closer to the desired frequency characteristic is used as the output of the recording apparatus, so that the output data series having the desired frequency characteristic is obtained.

Fig. 2 shows examples of input data series by interleaved NRZI at m=10, SB A, and output data series. As the polarity of SB A is inverted, the polarity of the second bit ahead of SB A is inverted according to formula (1). As the polarity of the second bit ahead of SB A is inverted, the polarity of the second bit ahead of the second bit ahead of SB A is inverted. In this way, as the polarity of SB A is inverted, the polarity of every odd-number bit counting from SB A is inverted. This inversion continues until the odd-number bit from SB A is a new SB, that is, SB C. In other words, by inverting the polarity of a certain SB, the polarity of the odd-number bit counting from that SB is inverted m times. The bit of (m+1) counting is a new SB C, and this inversion is not propagated. The bits inverted as SB A is inverted are m+1 bits indicated by bullet mark.

By such interleaved NRZI and propagation of change of SB polarity, changes of frequency characteristics by SB polarity change are increased.

Conventionally, the frequency components were compared between the bit row of m+1 bits by interleaved NRZI modulation with "0" added as SB to m bits, and the bit row of m+1 bits by interleaved NRZI modulation with "1" added as SB to m bits, and by recording m+1 closer to the frequency component of the desired frequency, the desired frequency component of recorded signal was controlled. As the means for extracting frequency components, Fourier transform is used.

It is hence a primary object of the invention to realize a circuit for controlling the frequency characteristics of digital signals by varying the polarity of SB to be inserted due to change of frequency characteristics of the bit varying in polarity by changing the bit to be inserted when modulating by interleaved NRZI by inserting one bit in every m bits, by a simple circuit (small-scale circuit).

To achieve the above object, the invention presents recording apparatus comprising bit extracting means for extracting inverted m+1 bits of a first series of bits obtained by interleaved NRZI modulation of an input data series added with one "0" bit per every m bits (m is 2 or larger even number) and a second series of bits obtained by interleaved NRZI modulation of the input data series added with one "1" bit per every m bits, frequency component extracting means for extracting at least two specified frequency components of the bit extracting means, output selection means for producing output bit series depending on the size of the frequency component, and recording means for recording output bit series in a magnetic tape.

Further features and advantages of the present invention will become clear from the following description of embodiments thereof, given by way of example, and illustrated by the accompanying drawings, in which:

Fig. 1 is a block diagram of an embodiment of the invention.

Fig. 2 is an explanatory diagram of interleaved NRZI modulation.

Fig. 3 is a block diagram of a bit extracting circuit 1.

Fig. 4 is a block diagram of a pre-coder 2.

Fig. 5 is a block diagram of other constitution of the embodiment.

Fig. 6 is a block diagram of an inverting circuit.

Fig. 7 is a block diagram of an output selecting circuit 5.

Fig. 8 is a block diagram of a pre-coder 14.

Fig. 9 is a block diagram of a different constitution of the embodiment.

Fig. 10 is a block diagram of a bit extracting circuit 17.

Fig. 11 is a block diagram of an output selecting circuit 18.

Fig. 12 is a block diagram of other constitution of the bit extracting circuit.

Fig. 13 is a block diagram of a bit dividing circuit 20.

Fig. 14 is a block diagram of a judging circuit 3.

Fig. 15 is a block diagram of IIR type digital filter

Fig. 16 is a block diagram of digital filters 23 and 24.

Fig. 17 is a block diagram of other constitution of the digital filters 23 and 24.

Fig. 18 is a block diagram of a representative value generating circuit 31.

Fig. 19 is a block diagram of a different constitution of the digital filters 23 and 24.

Fig. 20 is a frequency characteristic diagram of digital filter

Fig. 21 is a frequency characteristic diagram of digital filter.

Fig. 22 is a frequency characteristic diagram of recording signal.

Fig. 23 is a track pattern diagram.

Fig. 2 shows the relation between input data series and pre-coder output series in interleaved NRZI modulation. In every m bits of input data series, SB is inserted by one bit. By the pre-coder, the input data series is pre-coded according to formula (1). Therefore, when the polarity of SB is inverted, the odd-number bit counting from the SB is inverted. When the polarity of SB A is inverted, the odd-number bit from SB A is inserted, but the bits after SB C are determined by SB C, and the polarity of the bit after SB A by SB A influences only m+1 bits indicated by bullet mark bit in the pre-coder output series in Fig. 2. The circle mark bits do not depend on the polarity of SB A.

Hitherto, in the unit of m+1 bits starting from SB, the frequency component was extracted and the SB was determined. According to this method, when the polarity of the SB A is inverted, among m+1 bits to be noticed, the polarity is inverted in m/2+1 bits indicated by bullet mark, but the polarity is not inverted in m/2 bits indicated by circle mark. That is, m/2 bits are fixed bits not inverted by the polarity of SB A. By the presence of these fixed bits, change of frequency component by inversion of SB is blocked, which results in interference for obtaining a bit row possessing a desired frequency characteristic. In m/2 bits in next word, there are bits inverted in polarity by inversion of the polarity of SB A, but this interval is not taken into consideration for calculation of frequency components. Therefore, by performing the calculation of frequency components only in the SB and the bits influenced by this SB, the change of frequency characteristic by polarity change of SB can be increased, so that the notch or pilot of excellent characteristic may be generated.

This is to extract the bits influenced by the SB are extracted in the pre-coded series, but it is also possible to extract the bits to be influenced by the SB preliminarily from the series to be pre-coded or the input data series, and pre-code the selected bit row.

By calculating the frequency components of bullet marked bits only in Fig. 2, the number of bits to calculate the frequency components is m+1 bits, which is same as in the prior art, and the circuit scale for frequency component calculation is unchanged. Besides, by inversion of SB, all bits used in frequency component extraction are inverted, and therefore the pre-coded data when SB is "0" can be determined by inverting the pre-coded data when the SB is "1", and it is not necessary to determine the both pre-coded data when the SB is "0" and when the SB is "1", so that the circuit scale may be further curtailed.

One of the embodiments of the invention is described below with reference to accompanying drawings. Fig. 1 is a block diagram of an embodiment of the invention. In Fig. 1, numeral 1 is an A/D converter, 2 is a bit extracting circuit, 3a, 3b are pre-coders, 4 is a judging circuit, 5 is an output selecting circuit, 6 is a recording amplifier, 7 is a recording head, and 8 is a magnetic tape. An input video signal is sampled and quantized in the A/D converter 1, and is converted into a digital bit series $\{e_k\}$. This bit row is divided in every m bits, and an SB is inserted between them, and interleaved NRZI modulation is effected, and the bit series to be recorded $\{d_k\}$ is obtained, and by noticing a certain SB, in the bit extracting circuit 2, in order to determine this SB, m/2 even-number bits among next m bits from the place of insertion of the SB of notice in the output bit series of the A/D converter 1, and m/2 odd-number bits out of the next m bits are sent out to the pre-coders 3a and 3b. The bit row of m bits produced from the bit extracting circuit 1 comprises the bits influenced by the polarity of SB when modulated by interleaved NRZI. These bit rows (a_n (n = 0, 1, ..., m-1)) are prefixed by SB by the pre-coders 3a, 3b, modulated by interleaved NRZI, and sent out to the judging circuit 4 as bit rows of m+1 bits. Herein, the pre-coder 3a adds "0" as SB, and produces bit rows b_n (n = 0, 1, ..., m), while the pre-coder 3b adds "1" as SB, and produces bits $b_{n'}$ (n = 0, 1, ..., m). In the judging circuit 4, comparing the frequency characteristics of b_n and $b_{n'}$, the bit row closer to the desired frequency characteristic is judged, and the judged SB is sent out to the output selecting circuit 5. In the output selection circuit 5, the SB judged by the judging circuit 4 is inserted in every m bits of output series $\{e_k\}$ of the A/D converter 1, and interleaved NRZI modulation is performed, and the record bit row $\{d_k\}$ is sent to the recording amplifier 6. In the recording amplifier 6, the record bit row $\{d_k\}$ is converted into recording current, and is sent out into the recording head 7. In the recording head 7, the record bit row is recorded in the magnetic tape 8.

A block diagram of the bit extracting circuit 1 is shown in Fig. 3. The bits changed in polarity by SB polarity are bullet marked bits in the input data series shown in Fig. 2. Accordingly, the input data series $\{e_k\}$ is fed into a shift register 9, and when the next bit from the place for inserting the SB at the beginning comes, the even number bits of next m bits from the SB inserting place, and the odd number bits of second bit therefrom are produced. These bits are a_n.

In the pre-coders 3a, 3b, the input bit rows are precoded. The pre-coders 3a, 3b produce the input SB as b_0 as shown in Fig. 4, and operate a0 by exclusive OR with SB in an EXOR 10, and produce b1. This output, that is, b1 is operated by exclusive OR with a1 in the EXOR 10, and b2 is output. Thus, a_p is produced as b_{p+1} by exclusive OR with b_p (p = 0, 1, ..., m-1). At this time, the pre-coder 3a receives SB as 0, and produces bit row b_n. The pre-coder 3b receives SB as 1, and produces bit row $b_{n'}$.

Herein, between the output bit row of the pre-coder 3a when the SB is 0, and the output bit row of the pre-coder 3b when the SB is 1, as mentioned above, there is a relation in which all bits are mutually inverted, and hence, without using two pre-coders as in Fig. 1, by inverting the output b_n of the pre-coder 3a by an inverting circuit 11 as shown in Fig. 5, the same as the output b_n of the pre-coder 3b is obtained. Likewise, by generating the bit row b_n' by using the pre-coder 3b, the bit row b_n may be generated by inverting it. Or, by using one pre-coder in time sharing, b_n and $b_{n'}$ can be generated. Moreover, since b_0 is delivered to the judging circuit but b_0 is always 0 and $b_{n'}$ is always 1, they may be generated in the judging circuit 4 without producing outputs.

A block diagram of an inverting circuit 11 is shown in Fig. 6. An inverting element 12 produces 1 when the input bit is 0, and produces 0 when the input bit is 1. By feeding the bits of the bit row b_n into the inverting element 12, all bits are put out in inverted form. The output bit row is a same bit row as $b_{n'}$. Thus, b_n and $b_{n'}$ are generated.

The b_n and $b_{n'}$ are fed into the judging circuit 4, and the bit row closer to the specified frequency characteristic is judged, and the judged SB is put out. The judged SB is fed into the output selecting circuit 5. In the output selecting circuit 5, the bit series $\{e_k\}$ is entered. A block diagram of the output selecting circuit 5 is shown in Fig. 7. The bit series $\{e_k\}$ is fed into a delay circuit 13, and it is delayed until the SB is judged in the judging circuit 4. The output of the delay circuit 13 is fed into a pre-coder 14, and the judged SB is inserted in every m bits, and the pre-coded output is produced. The pre-coder 14 is composed, for example, as shown in Fig. 8, and the SB judged by the judging circuit 5 is inserted by a switch 15 in every m bits of the input bit series $\{e_k\}$. The bits delayed by the delay circuit 16 from the output series of the pre-coder 14, and the output bits of the switch 15 are operated by exclusive OR in an EXOR 17, and the result is produced as the output of the pre-coder 14. Herein, the delay circuit 16 and EXOR 17 are the circuits for realizing formula (1). The delay circuit 16 delays by one clock. The record bit series $\{d_k\}$ which is the output of the output selecting circuit 5 is converted into a recording current by the recording amplifier 6, and recorded in the magnetic tape 8 by the recording head 7.

Incidentally, the record bit series $\{d_k\}$ may be also produced as the record bit series $\{d_k\}$ by restructuring the pre-coded outputs b_n and $b_{n'}$ of the pre-coders 3a and 3b according to the determined SB, without precoding the $\{e_k\}$ newly.

In the foregoing description, the SB is judged by extracting the bits, that is, a_n of the input data series changed in the polarity by varying the polarity of SB, in the bit extracting circuit 2. By contrast, the SB may be preliminarily inserted as 0, and pre-coded, and bits changing in the polarity in the pre-coded series can be extracted. A block diagram at this time is shown in Fig. 9. The input data series is fed into a pre-coder 18, the SB is inserted as 0, and the interleaved NRZI modulation is performed. The output of the pre-coder 18 is fed into a bit extracting circuit 19, and bits changing in polarity by the change of SB polarity are extracted. The extracted bits are the same bit rows as the output, or b_n of the pre-coder 3a when the SB is 0. The output of the bit extracting circuit 19 is fed into the inverting circuit 11, and the pre-coded output $b_{n'}$ when the SB is 1 is produced. Both b_n and $b_{n'}$ are fed into the Judging circuit 4, and the bit row closer to the desired frequency characteristic is judged, and the judged SB is produced. The judged SB is fed into an output selecting circuit 20. In the output selecting circuit 20, from the judged SB and output series of the pre-coder 18, the recording bit series is delivered. The recording bit series is converted into a recording current by the recording amplifier 6, and recorded in the magnetic tape 8 by the recording head 7.

The pre-coder 18 is the same circuit as the pre-coder 14. However, always "0" is inserted as the SB. An example of the bit extracting circuit 19 is shown in Fig. 10. The bits to be inverted as the SB is inverted in the pre-coder output series b_n are, as shown in Fig. 2, m+1 bits including the SB of the odd number counting from the SB. The input pre-coder output series is fed into a shift register 21 of 2m+1 stages, and when the SB comes to the beginning of the shift register 21, m+1 bits are delivered in every 2 bits. This is the bit row pre-coded when the SB is 0, that is b_n, and it is fed in the judging circuit 4, and is also fed into the inverting circuit 11, thereby generating $b_{n'}$. The output $b_{n'}$ of the inverting circuit 11 is also put into the judging circuit 4. An example of output selecting circuit 20 is shown in Fig. 11. The output series of the pre-coder 18 in Fig. 9 is fed into the delay circuit 22, and is delayed until the SB is judged in the judging circuit 4. The SB determined to be the output series of the delay circuit 22 is fed into an EXOR 23. That is, what is fed into the output selecting circuit 18 is the pre-coder output series when the SB is "0", and nothing is delivered when the determined SB corresponding to the output bit is "0", and when the determined SB is "1", it is inverted and put out.

Instead of the record bit series $\{d_k\}$, the determined SB may be inserted into the input data series $\{e_k\}$, and precoded, and the record bit series $\{d_k\}$ may be obtained.

The bit extracting circuit 2 may be composed without using the shift register. A block diagram of the bit extracting circuit 2 at this time is shown in Fig. 12.

The data series $\{e_k\}$ entered in m-bit parallel data is fed into a bit dividing circuit 24, and is divided into odd-number bits and even-number bits from the beginning. An example of the bit dividing circuit 24 is shown in Fig. 13. The odd-number bits divided by the bit dividing circuit 24 are fed into the delay circuit 21. The output bit row of a delay circuit 25 and the even-number bit output of the bit dividing circuit 24 are nothing but a_n. In such constitution, the circuit scale may be further reduced for the data series of parallel input.

In such constitution, by extracting the bit row changing in the polarity by varying the SB polarity, and determining the SB by comparison of frequency components of the bit rows, bit series of larger notch or larger pilot may be generated and recorded. In this method, the number of bits of the bit row used in the judgement of SB is unchanged, that is, m+1 bits, and the recording apparatus may be composed in a similar circuit scale.

To judge the SB, hitherto, the frequency component was extracted by using Fourier transform. For Fourier transform, however, it was necessary to multiply the input series by the sine and cosine waveforms as the reference. As known well, the multiplier is large in circuit scale, which caused to increase the cost of the circuit for extracting the frequency component. In addition, to determine the frequency component, the square mean of the determined sine component and cosine component must be calculated. It is also large in the circuit scale, leading to increase of cost of the circuit for extracting the frequency component.

To solve these problems, it is possible to extract the frequency components by using digital filter. Fig. 14 shows a block diagram of the judging circuit 4 using digital filters for extracting the frequency components for judging the SB. In digital filters 26 and 27, the frequency components of the input bit series are extracted by using the digital filters of IIR (Infinite Impulse Response) type. Herein, notches are provided at two frequencies f_1 and f_2, and the f_1 frequency components of b_n and $b_{n'}$ are determined in the digital filter 26, and the f_2 frequency components of b_n and $b_{n'}$ are determined in the digital filter 27. The f_1 frequency component and f_2 frequency component of b_n determined in the digital filters 26 and 27 are added in an adder 28a, and fed into a comparator circuit 29. Similarly, the f_1 frequency component and f_2 frequency component of $b_{n'}$ are added in an adder 28b, and fed into the comparator circuit 29. In the comparator circuit, the frequency components of b_n and $b_{n'}$ are compared, and the smaller SB is delivered as the determined SB. The determined SB is fed into the digital filters 26, 27 in order to match with the internal data of the digital filters. When adding the pilot component to the frequency of f_0, before input of b_n and $b_{n'}$ to the digital filters 26 and 27, $\sin 2\pi f_0 t$ is added by the adder 25a and adder 25b, the series of the frequency characteristic possessing pilot component and also having notch can be selected. In the adder 25a, b_n and $\sin 2\pi f_0 t$ are added, and in the adder 25b, $b_{n'}$ and $\sin 2\pi f_0 t$ are added. Herein is shown a block of judging circuit for selecting the series in which notches are provided in the frequencies of f_1 and f_2 and there is a pilot in the frequency of f_0, but selection of bit series having notches in more frequencies is possible to parallel connection of a digital filter for extracting the frequency component with the digital filters 26 and 27. The pilot frequency is f_0, but it may be the same frequency as f_1 or f_2.

A block diagram of general IIR type digital filters is shown in Fig. 15. The outputs of digital filters are delayed in a delay circuit 32, a coefficient is multiplied in a multiplier 31, and input data series is added, and the sum is output. By varying the number of stages of the delay circuit 32 and the coefficient of the multiplier 31, it is known that a filter possessing an arbitrary frequency characteristic. The digital filter 26 and digital filter 27 extract the frequency components of f_1 and f_2 according to the principle of the IIR type digital filter. In this constitution, a delay circuit 32 is an element for delaying the bit clock of 1 bit.

A block diagram of the digital filter 26 is shown in Fig. 16. An adder 33a, delay circuits 32, 34 and 34a, and multiplier 31a compose an IIR type digital filter having the peak at the frequency of f_1 to b_n. The output of the adder 33a is combined with the sum of the frequency components hitherto recorded in a register 37a by the adder 36a, and an absolute value is obtained in the absolute value circuit 35a, and the f_1 frequency component of b_n is delivered. Similarly, an adder 33b, delay circuits 32, 34, 34b, and multiplier 31b compose an IIR type digital filter having the peak at the frequency of f_1 to $b_{n'}$, and produce an output. The output of the adder 33b is combined with the sum of the frequency components hitherto recorded in a register 37b by the adder 36b, and an absolute value is obtained in the absolute value circuit 35b, and the frequency component of f_1 of $b_{n'}$ is produced.

In this way, the frequency components of b_n and $b_{n'}$ are calculated and produced. The delay component of the digital filter when the SB is 0 is delayed in the delay circuit 34a, and when the SB is 1 in the delay circuit 34b. Accordingly, when the SB is determined by the frequency components of outputs b_n and $b_{n'}$, if the determined SB is 0, the content of the delay element 34a is copied in the delay circuit 34b. If the determined SB is 1, to the contrary, the content of the delay element 34b is copied in the delay circuit 34a. Similarly, the contents of the registers 37a and 37b are copied according to the determined SB. Thus, regardless of the determined SB, matching of digital filters is achieved.

In Fig. 16, the digital filter 26 is explained, whereas the digital filter 27 is composed by constructing the IIR type digital filter having the peak at f_2 by varying the number of stages of the delay circuit 32 in Fig. 15 and coefficients of the multipliers 31a and 31b.

In this way, the frequency components can be operated by using the digital filters. This method is not practical because lots of calculations are necessary in each bit. Hence, without having to calculate the frequency components in every bit, by determining a representative value in every specific bits, and determining the frequency component of the representative value, the frequency components of bit row can be determined. A block diagram of the digital filter 26 in this case is shown in Fig. 17. The input b_n is put into a representative value generating circuit 38a, and $b_{n'}$ into a representative value generating circuit 38b, and the representative value of every k bits (k is a natural number) is generated and produced. The adder 33a, delay circuits 40, 39, 39a, and multiplier 31a compose an IIR digital filter having the peak at f_1, and the frequency component of f_1 of the representative value of the input b_n is produced. Similarly, the adder 33b, delay circuit 40, 39 and 39b, and multiplier 31b composed an IIR type digital filter having the peak at f_1, and the frequency component of f_1 of the representative value of the input $b_{n'}$ is produced. The output of the adder 33a is combined with the value of the register 37a,the absolute value is obtained by the absolute value circuit 35a, and produced as the frequency component of f_1 of b_n. Similarly, the output of the adder 33b is combined with the value of the register 37b, and the absolute value is obtained by the absolute value circuit 35b, and is produced as the frequency component of f_1 of $b_{n'}$. Same as in the digital filter 26 shown in Fig. 16, when the SB is determined, the value determined by the delay circuits 39a and 39b, or registers 37a and 37b is copied in the other delay circuit or register.

As an example of representative value produced by the representative value generating circuit, DSV (digital sum variation) may be employed. A block diagram of the representative value generating circuit for generating DSV as representative value is shown in Fig. 18. The DSV is obtained by integrating "0" of bit row as -1,and "1" as +1. The DSV is stored in the register 42. In the adder 41, converted into the input bit +1 or -1, it is combined with the DSV stored in the register 41, and the sum is stored a register 42. After addition of k-th bit, the DSV of the calculation result is combined with the stored DSV, and produced as output. The DSV generated here is the DSV corresponding to the input series. After the SB is determined, the value of the register 42 of the determined representative value calculating circuit is copied in the register 42 of the representative value calculating circuit.

In this circuit composition, as compared with the circuit composition in Fig. 16, the delay circuit and multiplier are required only by 1/k for extracting frequency components of the same frequency, and the circuit scale is reduced, and the operating speed can be slowed down, so that the energy may be saved.

In the circuit composition in Fig. 17, supposing the coefficients of the multipliers 31a and 31b of the final stage to be 1, and the coefficients of the other multiplies 31a and 31b to be 0, a block diagram of digital filter 24 is shown in Fig. 19.

Of the input bit row b_n, the representative value is generated and produced by the representative value generating circuit 38a. The representative value is fed into a digital filter composed of adder 33a, and delay circuits 43 and 44a. The output of the adder 33a is fed into the absolute value circuit 25a, and is produced as the f_1 frequency component of b_n. Similarly, of the input bit row $b_{n'}$, the representative value is generated and produced in the representative value generating circuit 38b. The representative value is fed into a digital filter composed of adder 33b and delay circuits 43 and 44b. The output of the adder 33b is fed into the absolute value circuit 25b, and produced as frequency components of f_1 of $b_{n'}$.

The frequency characteristic of the digital filter in Fig. 19 is shown in Fig. 20. The delay time of the delay circuit 43 is set so that the frequency to be extracted, or f_1, may be the lowest frequency of peak. When generating notches at plural frequencies, by varying the delay time of the delay circuit 43, it is possible to vary the frequency for generating notches. Such digital filters are arranged parallel as many as the number of notches, and the sums of the frequency components are compared, and the SB is determined.

Reviewing the frequency characteristics in Fig. 20, not only f_1 which is the desired frequency, but also the DC component at which the frequency is 0, and component of frequency of a common multiple of f_1 are produced by the digital filter in Fig. 19. Accordingly, when generating notches in two frequencies f_1 and f_2, by using the digital filter in Fig. 19 at the frequency of the greatest common measure of f_1 and f_2, the notches at frequencies f_1 and f_2 can be composed of one digital filter. Supposing the ratio of frequencies f_1 and f_2 to be 2:3, the frequency characteristic may be as shown in Fig. 21 by setting the fundamental frequency of digital filter to be $f_1/2$, and it is possible to set notches at two frequencies by using only one digital filter, which contributes to reduction of circuit scale.

Claims

1. A recording apparatus comprising bit extracting means for extracting inverted m+1 bits of a first series of bits obtained by interleaved NRZI modulation of an input data series added with one "0" bit per every m bits (m is 2 or larger even number) and a second series of bits obtained by interleaved NRZI modulation of the input data series added with one "1" bit per every m bits, frequency component extracting means for extracting at least two specified frequency components from outputs of the bit extracting means, output selection means for producing output bit series depending on a value of the frequency component, and recording means for recording the output bit series on a recording medium.

2. A recording apparatus of claim 1, wherein the bit extracting means comprises bit inserting means for inserting a bit of "0" or "1" in every m bits of the input data series, a pre-coder for modulating the output series of the bit inserting means by interleaved NRZI, and a shift register for delaying an output of the pre-coder and producing selected bits.

3. A recording apparatus of claim 1, wherein the bit extracting means comprises delay means for delaying even-number bits of the m bits of the input data series, and a pre-coder for adding odd-number bits of the input data series and a bit of "0" or "1" to an output of the delay means, and modulating by interleaved NRZI.

4. A recording apparatus comprising a digital filter for extracting at least two specified frequency components from a first series of bits obtained by interleaved NRZI modulation of an input data series added with one "0" bit per every m bits and a second series of bits obtained by interleaved NRZI modulation of the input data series added with one "1" bit per every m bits, output selecting means for producing output data series depending on a value of the frequency component, and recording means for recording the output data series on a recording medium.

5. A recording apparatus of claim 4, wherein the digital filter is a digital filter for extracting the frequency components at the frequency of a common measure of extracting frequency.

6. A recording apparatus comprising:
   representative value generating means for generating a representative value of every k bits of series,
   a digital filter for extracting at least two specified frequency components in the series of the representative values,
   output selecting means for producing output data series depending on values of frequency components, and
   recording means for recording output data series on a recording medium in a two-series system consisting of a series obtained by interleaved NRZI modulation of an input data series added with one "0" bit per every m bits and a series obtained by interleaved NRZI modulation of the input data series added with one "1" bit per every m bits.

7. A recording apparatus of claim 6, wherein the digital filter is a digital filter for extracting the frequency components at the frequency of a common measure of extracting frequency.

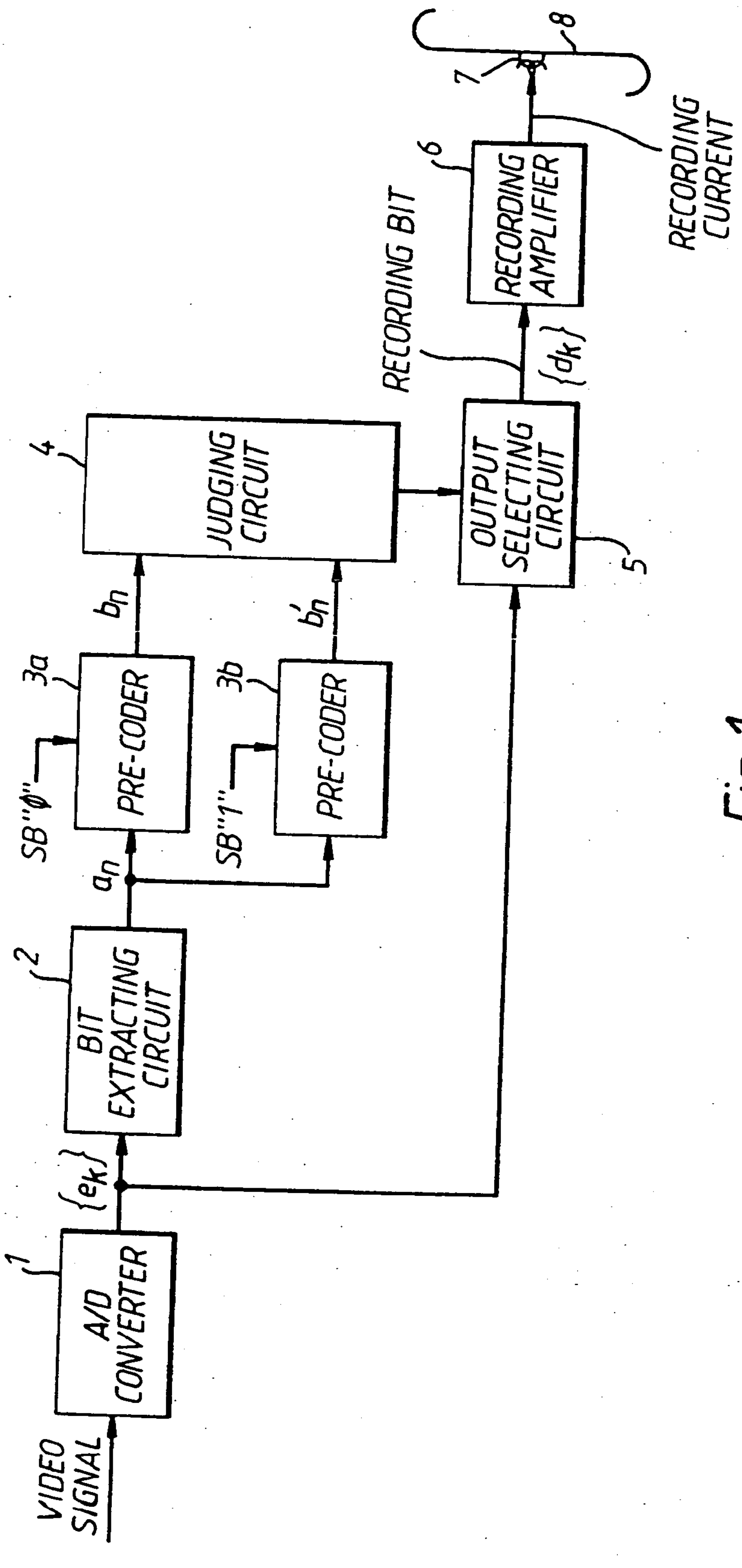

VIDEO SIGNAL
1
A/D CONVERTER
{ek}
2
BIT EXTRACTING CIRCUIT
an
SB"0"
3a
PRE-CODER
SB"1"
3b
PRE-CODER
bn
b'n
4
JUDGING CIRCUIT
OUTPUT SELECTING CIRCUIT
5
RECORDING BIT
{dk}
6
RECORDING AMPLIFIER
RECORDING CURRENT
7
8

Fig. 1

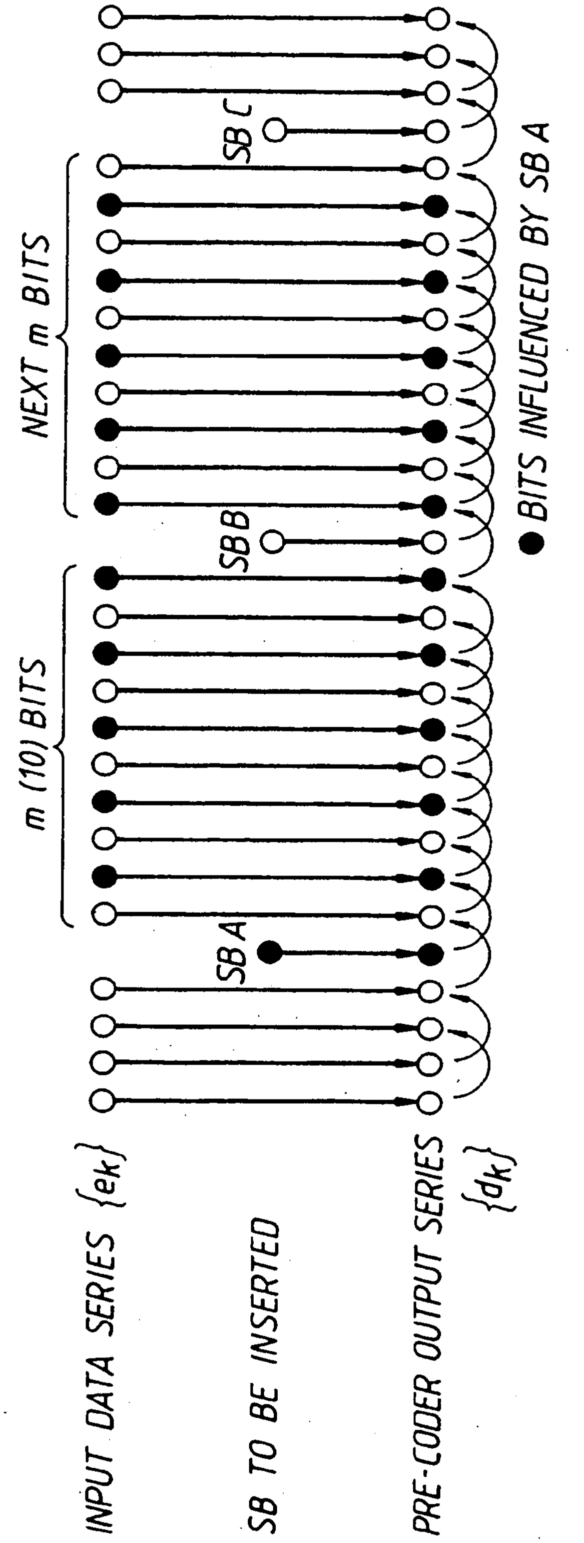

INPUT DATA SERIES {ek}
SB TO BE INSERTED
PRE-CODER OUTPUT SERIES {dk}
SB A
SB B
SB C
m (10) BITS
NEXT m BITS
● BITS INFLUENCED BY SB A

Fig. 2

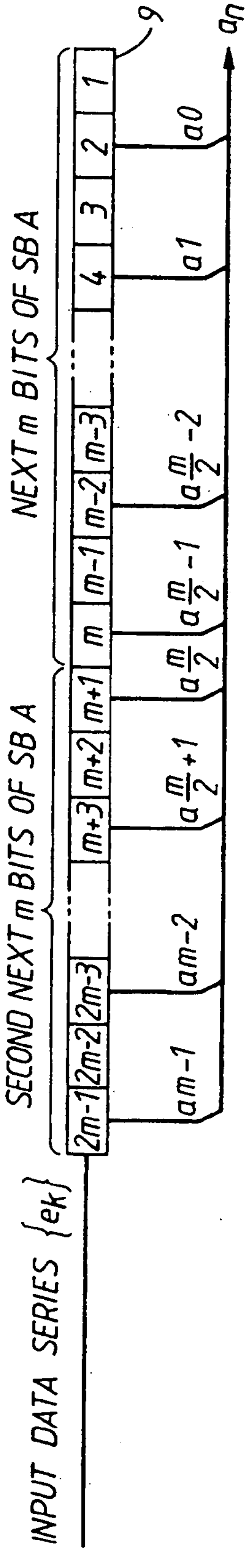

INPUT DATA SERIES {ek}
SECOND NEXT m BITS OF SB A
NEXT m BITS OF SB A
2m-1
2m-2
2m-3
m+3
m+2
m+1
m
m-1
m-2
m-3
4
3
2
1
9
am-1
am-2
a m/2 +1
a m/2
a m/2 -1
a m/2 -2
a1
a0
an

Fig. 3

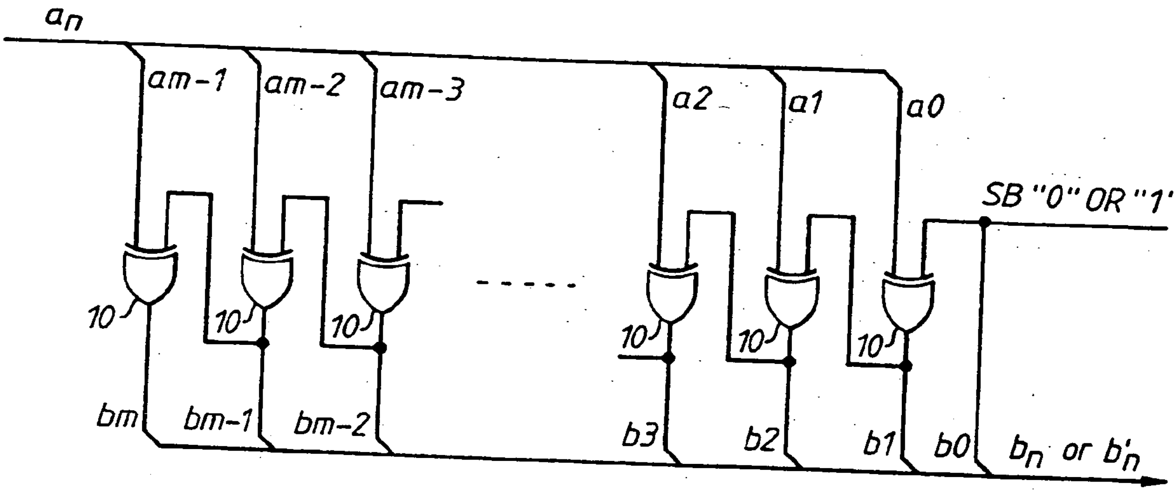

an
am-1
am-2
am-3
a2
a1
a0
SB "0" OR "1"
10
10
10
10
10
10
bm
bm-1
bm-2
b3
b2
b1
b0
bn or b'n

Fig. 4

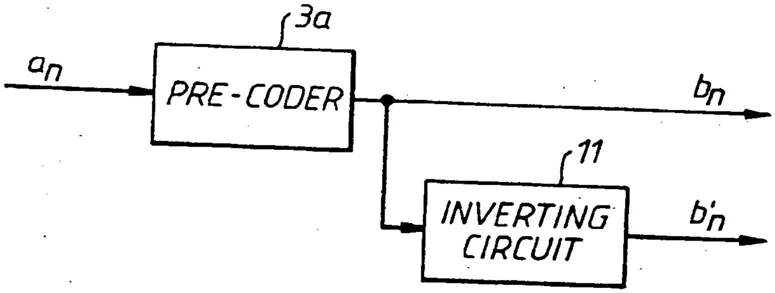

3a
an
PRE-CODER
bn
11
INVERTING CIRCUIT
b'n

Fig. 5

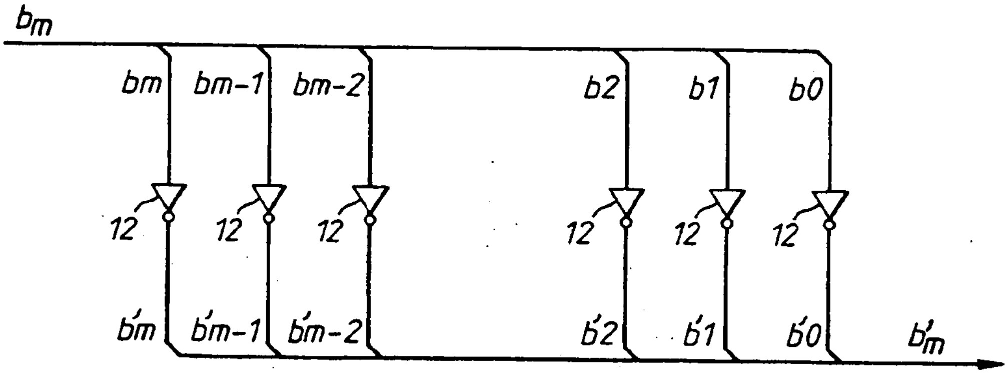


Fig.6

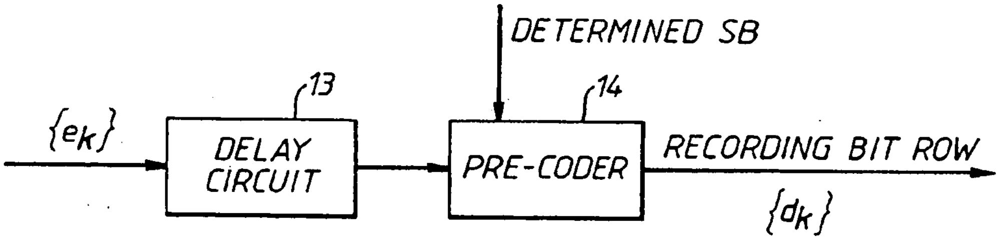


Fig.7

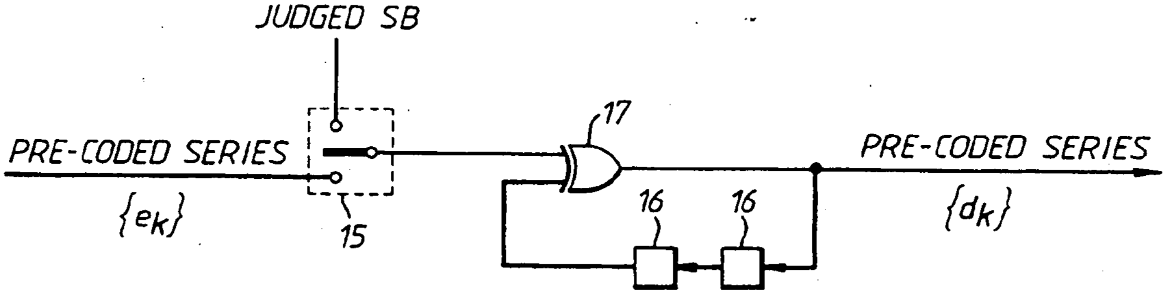


Fig.8

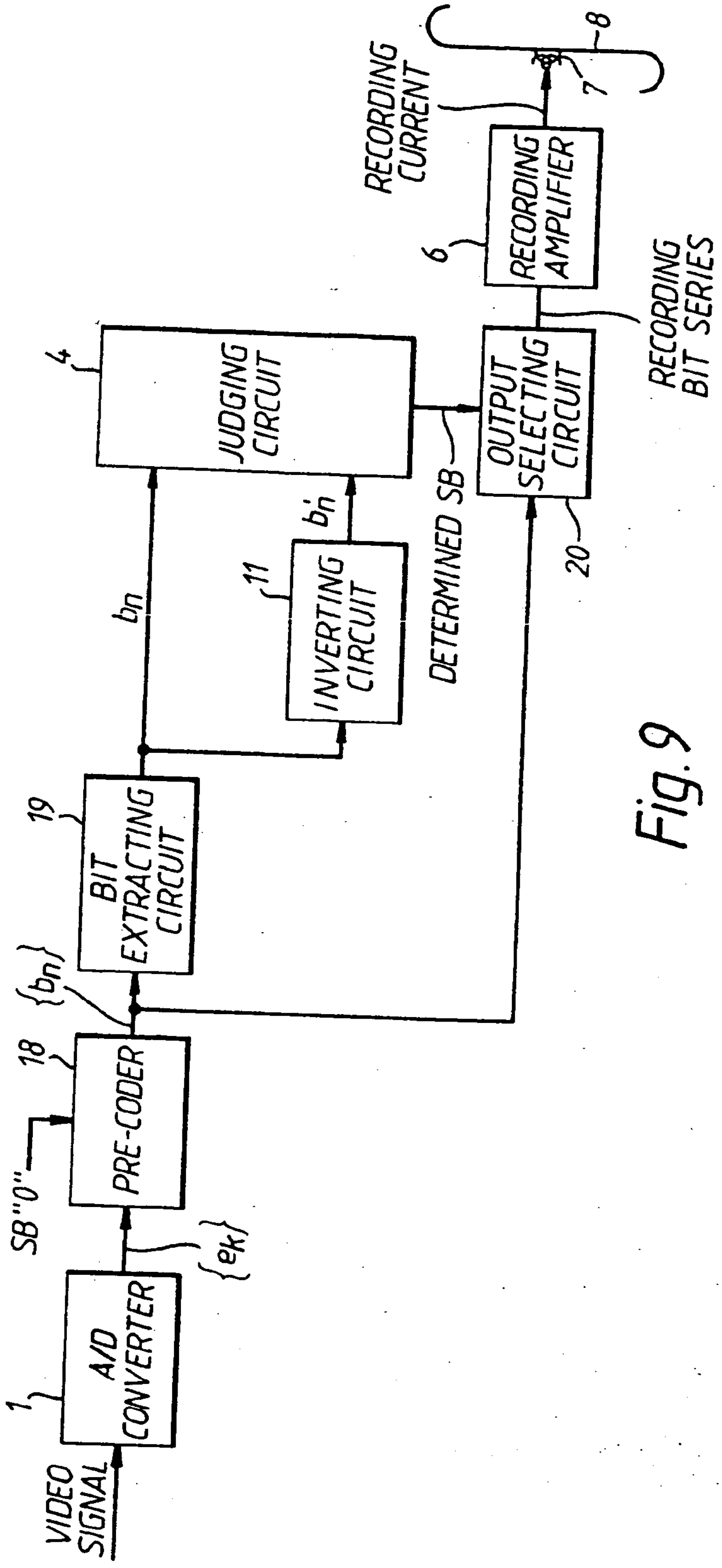

VIDEO SIGNAL
1
A/D CONVERTER
{ek}
SB"0"
18
PRE-CODER
{bn}
19
BIT EXTRACTING CIRCUIT
bn
11
INVERTING CIRCUIT
b̄n
4
JUDGING CIRCUIT
DETERMINED SB
20
OUTPUT SELECTING CIRCUIT
RECORDING BIT SERIES
6
RECORDING AMPLIFIER
RECORDING CURRENT
7
8

Fig.9

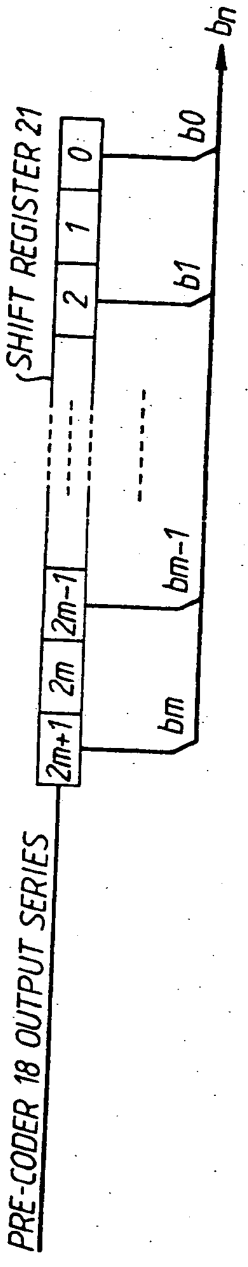

PRE-CODER 18 OUTPUT SERIES
SHIFT REGISTER 21
2m+1
2m
2m-1
2
1
0
bm
bm-1
b1
b0
bn

Fig.10

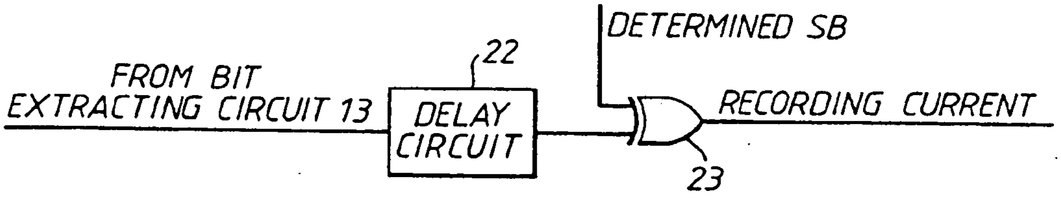


Fig.11

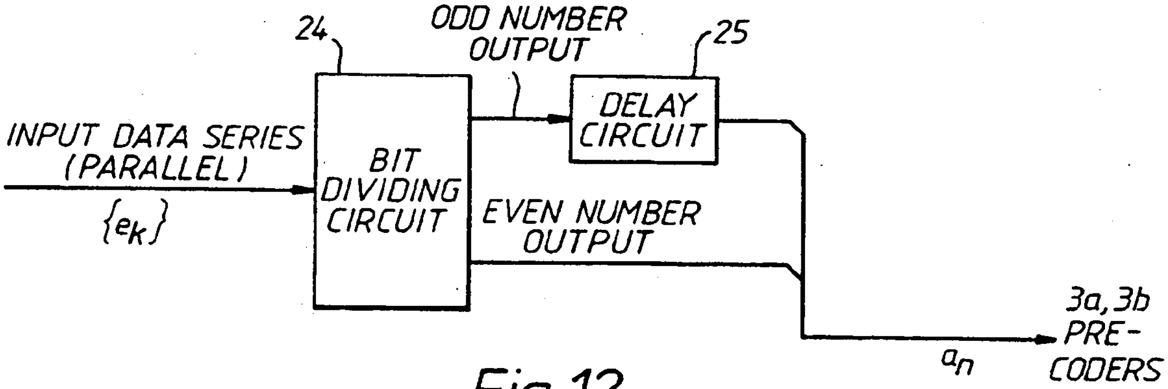


Fig.12

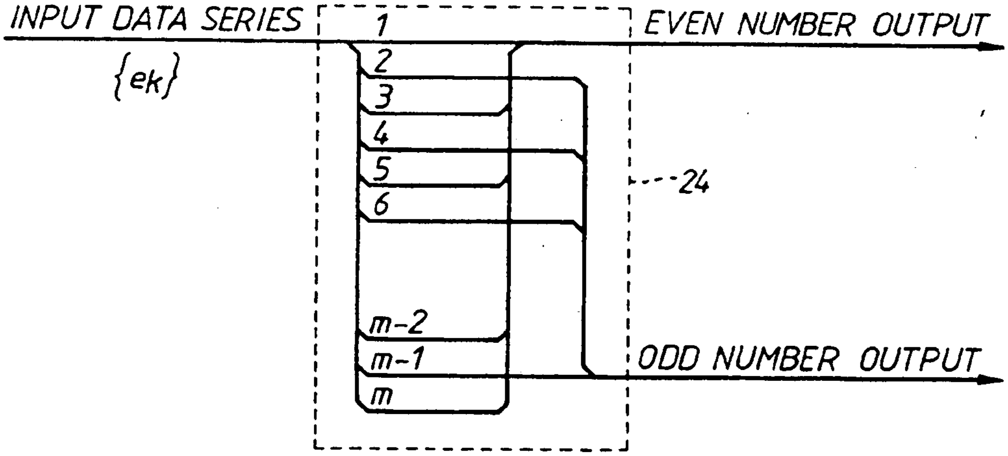


Fig.13

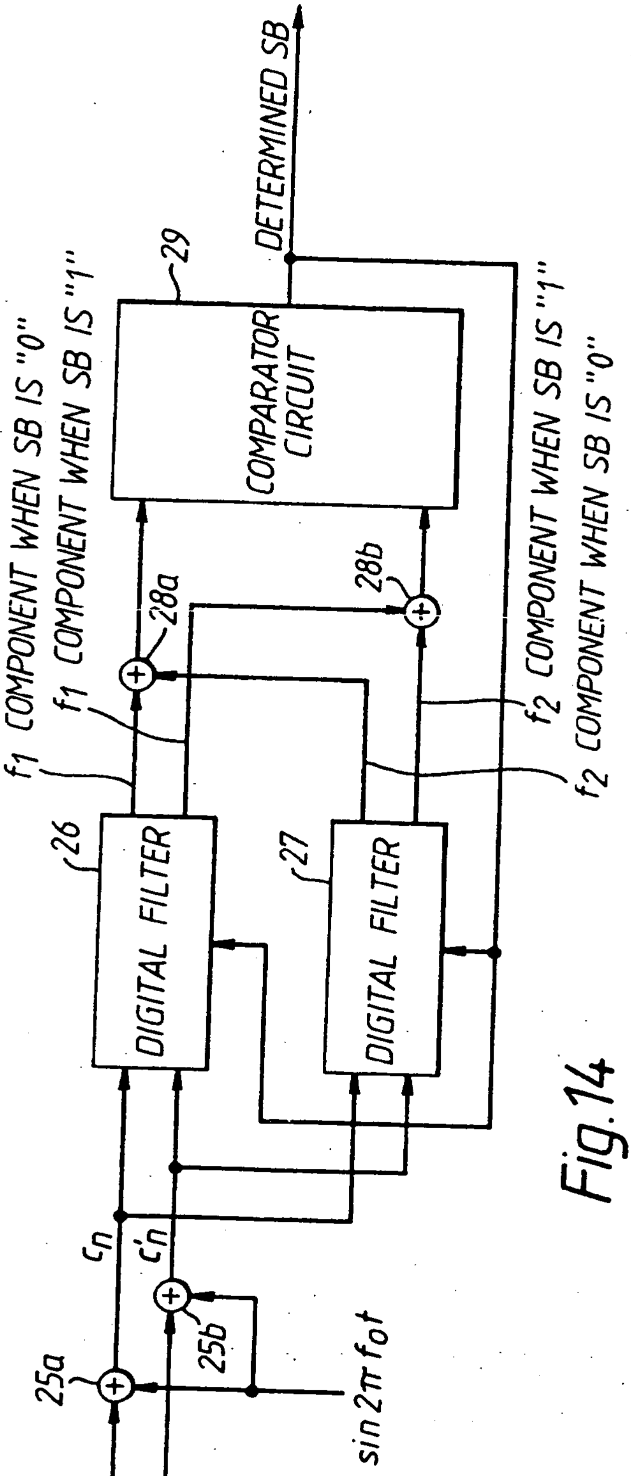

b_n
b'_n
25a
25b
$\sin 2\pi f_0 t$
c_n
c'_n
26
DIGITAL FILTER
27
DIGITAL FILTER
f_1
f_1 COMPONENT WHEN SB IS "0"
f_1 COMPONENT WHEN SB IS "1"
28a
28b
f_2 COMPONENT WHEN SB IS "1"
f_2 COMPONENT WHEN SB IS "0"
f_2
COMPARATOR CIRCUIT
29
DETERMINED SB

Fig.14

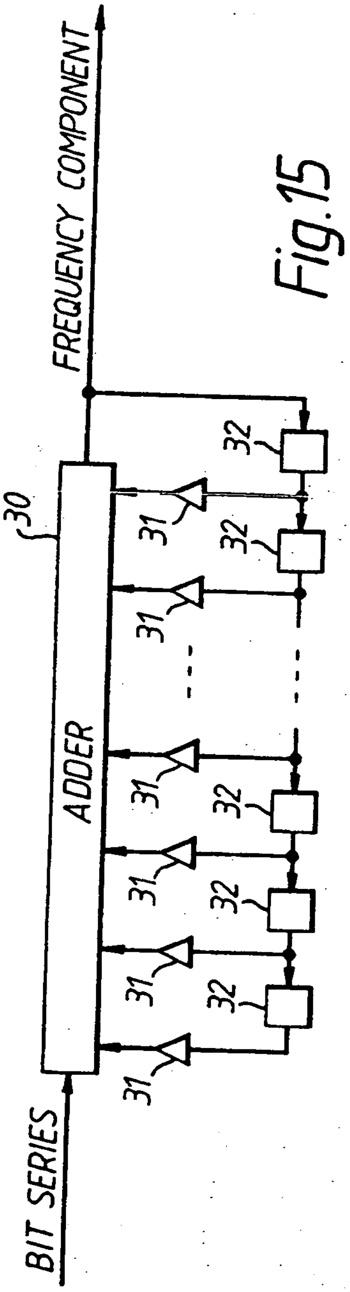

BIT SERIES
30
ADDER
31
32
FREQUENCY COMPONENT

Fig.15

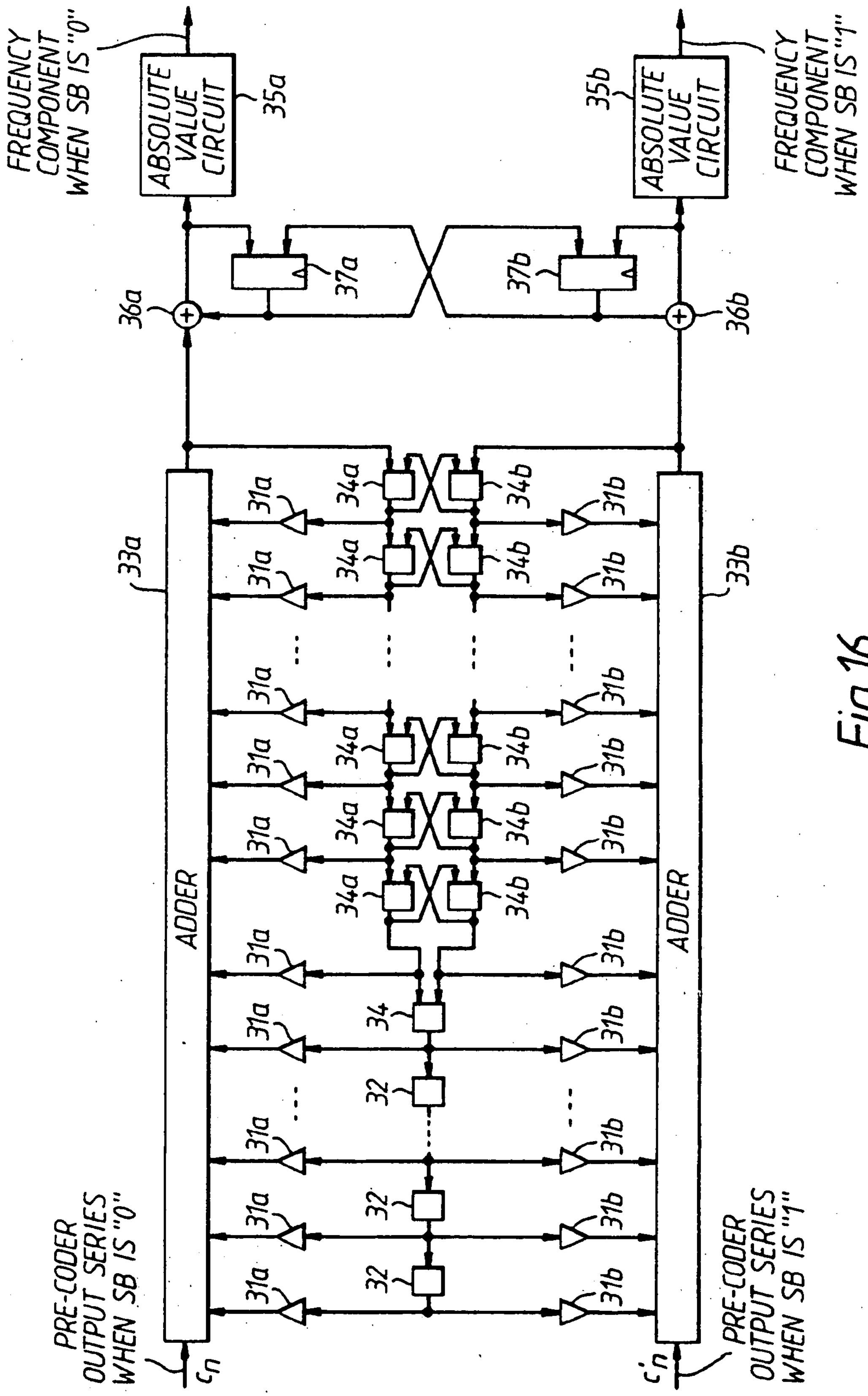

PRE-CODER OUTPUT SERIES WHEN SB IS "0"
c_n
PRE-CODER OUTPUT SERIES WHEN SB IS "1"
c'_n
ADDER
33a
ADDER
33b
31a
31b
32
34
34a
34b
36a
36b
37a
37b
ABSOLUTE VALUE CIRCUIT
35a
ABSOLUTE VALUE CIRCUIT
35b
FREQUENCY COMPONENT WHEN SB IS "0"
FREQUENCY COMPONENT WHEN SB IS "1"

Fig.16

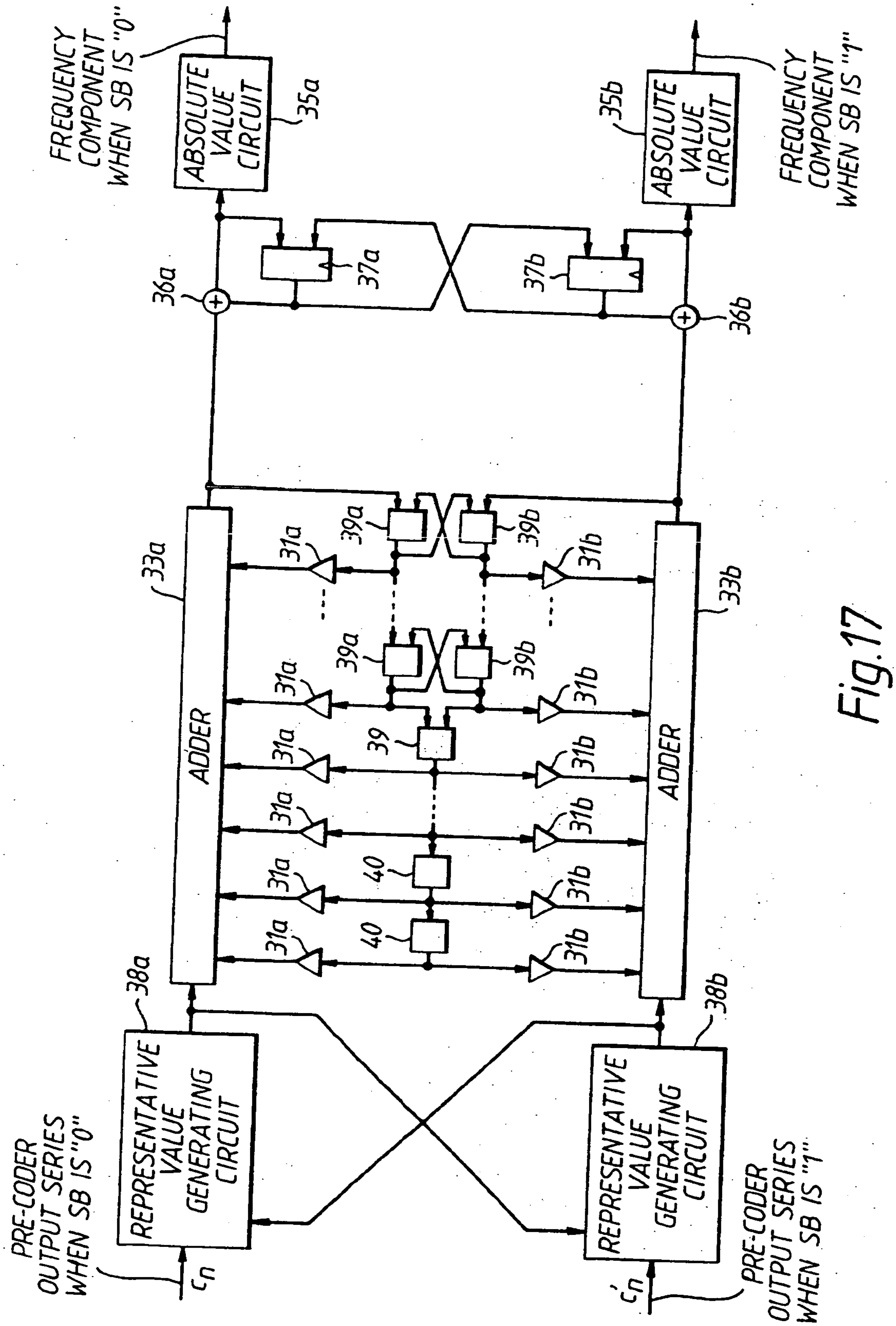

FREQUENCY COMPONENT WHEN SB IS "0"
ABSOLUTE VALUE CIRCUIT
35a
36a
37a
35b
ABSOLUTE VALUE CIRCUIT
FREQUENCY COMPONENT WHEN SB IS "1"
37b
36b
33a
ADDER
39a
39b
31a
31b
39
40
33b
ADDER
38a
REPRESENTATIVE VALUE GENERATING CIRCUIT
PRE-CODER OUTPUT SERIES WHEN SB IS "0"
c_n
38b
REPRESENTATIVE VALUE GENERATING CIRCUIT
PRE-CODER OUTPUT SERIES WHEN SB IS "1"
c'_n

Fig.17

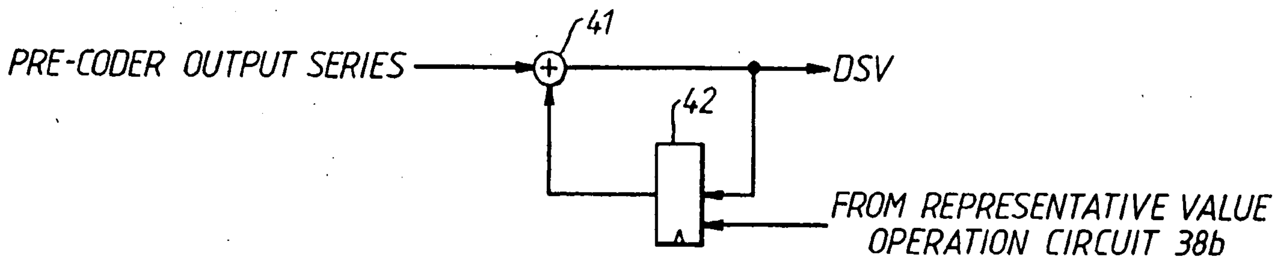

PRE-CODER OUTPUT SERIES
41
42
DSV
FROM REPRESENTATIVE VALUE
OPERATION CIRCUIT 38b

Fig.18

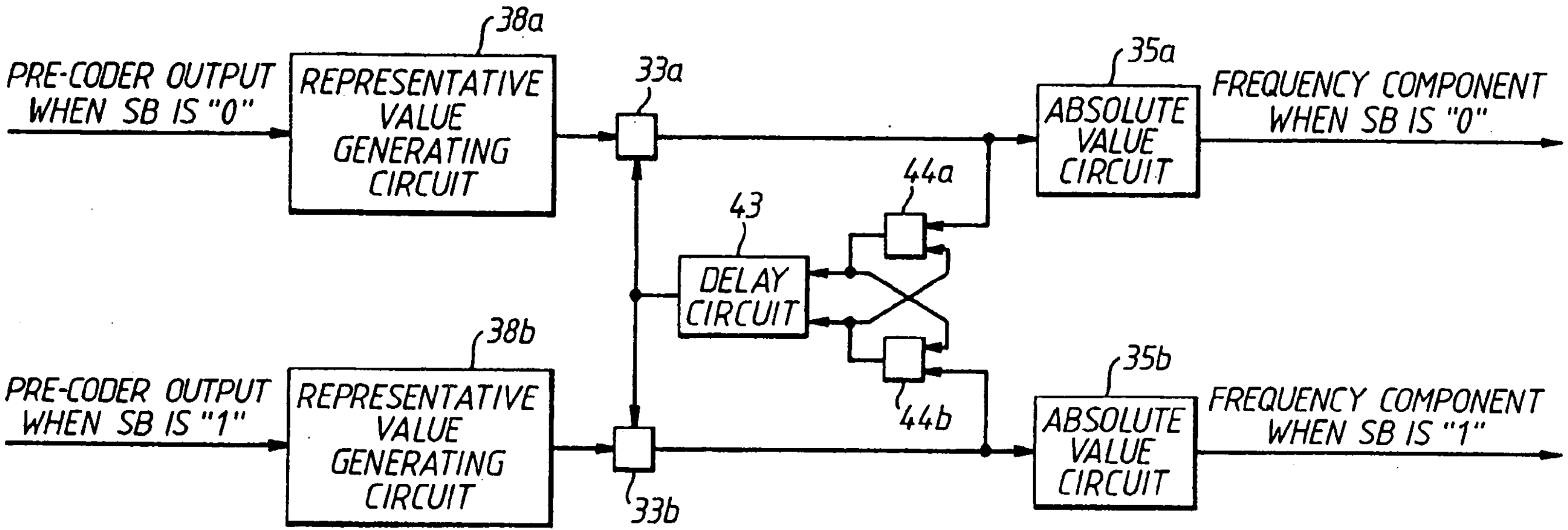

38a
PRE-CODER OUTPUT
WHEN SB IS "0"
REPRESENTATIVE
VALUE
GENERATING
CIRCUIT
33a
35a
ABSOLUTE
VALUE
CIRCUIT
FREQUENCY COMPONENT
WHEN SB IS "0"
44a
43
DELAY
CIRCUIT
38b
PRE-CODER OUTPUT
WHEN SB IS "1"
REPRESENTATIVE
VALUE
GENERATING
CIRCUIT
44b
35b
ABSOLUTE
VALUE
CIRCUIT
FREQUENCY COMPONENT
WHEN SB IS "1"
33b

Fig.19

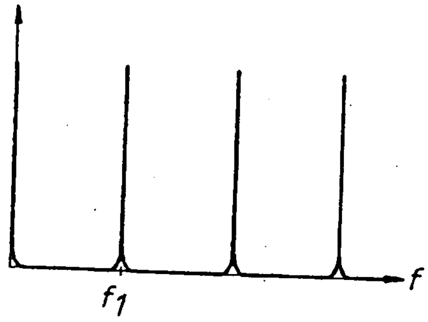
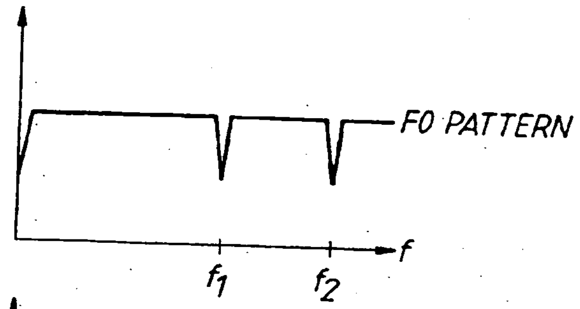


Fig. 20



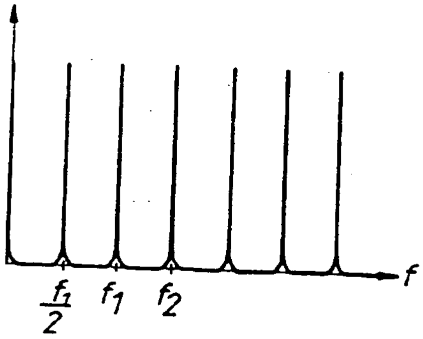


Fig. 21

Fig. 22

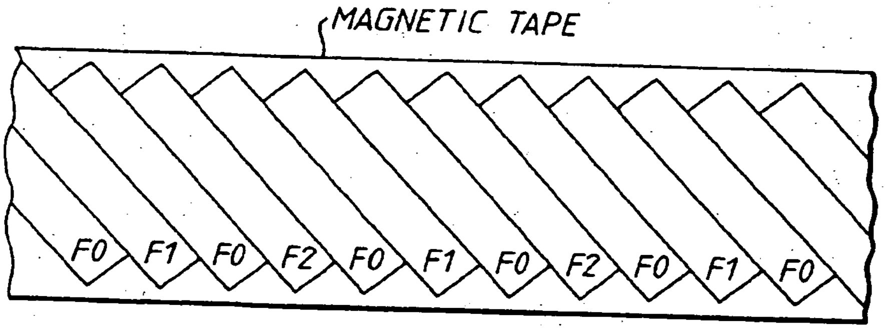


Fig. 23

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Office européen des brevets

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(30) Priority : **16.10.92 JP 278954/92**
01.12.92 JP 321608/92
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01.12.92 JP 321611/92

(43) Date of publication of application :
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16.08.95 Bulletin 95/33

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303-306 High Holborn
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(54) Apparatus for recording digital signals by controlling frequency characteristics of digital signals.

(57) When modulating by interleaved NRZI by inserting one bit per every m bits of input data series, the frequency characteristics of bit rows varying by the polarity ("0" or "1") of the bit to be inserted are compared. and the bit row closer to the desired frequency characteristic is selected as the output series, so that recording is effected by controlling the frequency characteristics of the digital signal.

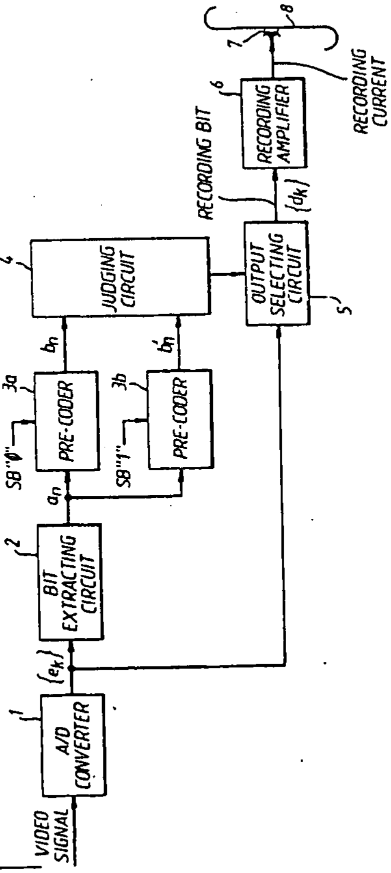

Fig.1

EP 0 593 173 A3

Jouve, 18, rue Saint-Denis, 75001 PARIS

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 93 30 7554

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
A	PATENT ABSTRACTS OF JAPAN vol. 017 no. 058 (P-1481) ,4 February 1993 & JP-A-04 268258 (MATSUSHITA ELECTRIC IND CO LTD) 24 September 1992, * abstract * ---	1,4,6	G11B20/14 //G11B15/46
A	PATENT ABSTRACTS OF JAPAN vol. 015 no. 308 (E-1097) ,7 August 1991 & JP-A-03 109823 (CANON INC) 9 May 1991, * abstract * ---	1,4,6	
A	PATENT ABSTRACTS OF JAPAN vol. 016 no. 404 (P-1410) ,26 August 1992 & JP-A-04 134758 (MATSUSHITA ELECTRIC IND CO LTD) 8 May 1992, * abstract * ---	1,4,6	
A	PATENT ABSTRACTS OF JAPAN vol. 010 no. 259 (E-434) ,4 September 1986 & JP-A-61 084124 (MATSUSHITA ELECTRIC IND CO LTD) 28 April 1986, * abstract * ---	1,4,6	TECHNICAL FIELDS SEARCHED (Int.Cl.5)
A	PATENT ABSTRACTS OF JAPAN vol. 010 no. 046 (E-383) ,22 February 1986 & JP-A-60 201728 (CANON KK) 12 October 1985, * abstract * ---	1,4,6	G11B
A	EP-A-0 339 724 (PHILIPS NV) 2 November 1989 * the whole document * ---	1-7	
A	EP-A-0 476 766 (PHILIPS NV) 25 March 1992 * the whole document * --- -/--	1-7	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	14 June 1995	Nanos, A

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A : technological background
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P : intermediate document

T : theory or principle underlying the invention
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D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 93 30 7554

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
A	EP-A-0 250 049 (PHILIPS NV) 23 December 1987 * the whole document * -----	1-7	
			TECHNICAL FIELDS SEARCHED (Int.Cl.5)

The present search report has been drawn up for all claims

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